Lab 07

Adder Design Tradeoffs

ECE 380-002

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**Introduction**

In this lab, we use the Quartus II software package to design and test combinational circuit designs with multiplexers and decoders. We understand standard IC chips 74151, an 8-to-1 multiplexer, and 74154, a 4-to-16 decoder and use them to implement logic functions.

**Procedure**

1. Prelab
2. Design A

A screenshot of a computer

Description automatically generatedIn the design A, we analyze the logic function by truth table. Then we implement the function to the multiplexer. Then stimulate the schematic file, which is same as we expect.

A screenshot of a video game

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1. Design B

In the design B, we also analyze the problem by created a 4-varible truth table. Then, we implement to the 4-to-16 decoder. Then we compile and simulate the file. The result is also matching our expected in the analyzing part.

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1. Chips description
2. Chip 74151

This chip is an 8-to-1 multiplexer with an enable input, three select signal inputs and 8 function input.

1. Chip 74154

This chip is a 4-to-14 encoder. The chip will enable by both enable switch is off. The take 4-varibles for input.

1. During the lab
2. Design A

A screenshot of a cell phone

Description automatically generatedIn the lab, we assign the input and the output to the pin. Then we compiled the file again and test on the DE1 board. The result is also correct our simulate result and expect result.

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1. Design B

We repeat the same process in the design A, the result is also same as our simulate result and our respect result.

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**Result**

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Description automatically generatedThe result is same as we expected and simulated result.

A close up of a piece of paper

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**Conclusion**

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Description automatically generatedIn the lab, we understand how to use multiplexer and decoder to implement logic functions and test the result on the DE1 board.